

MC100EP210S

2.5V 1:5 Dual Differential LVDS Compatible Clock Driver

Description

The MC100EP210S is a low skew 1-to-5 dual differential driver, designed with LVDS clock distribution in mind. The LVDS or LVPECL input signals are differential and the signal is fanned out to five identical differential LVDS outputs.

The EP210S specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

Two internal 50 Ω resistors are provided across the inputs. For LVDS inputs, VTA and VTB pins should be unconnected. For LVPECL inputs, VTA and VTB pins should be connected to the V_{TT} ($V_{CC} - 2.0$ V) supply.

Designers can take advantage of the EP210S performance to distribute low skew LVDS clocks across the backplane or the board.

Features

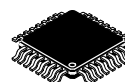
- 20 ps Typical Output-to-Output Skew
- 85 ps Typical Device-to-Device Skew
- 550 ps Typical Propagation Delay
- The 100 Series Contains Temperature Compensation
- Maximum Frequency > 1 GHz Typical
- Operating Range: $V_{CC} = 2.375$ V to 2.625 V with $V_{EE} = 0$ V
- Internal 50 Ω Input Termination Resistors
- LVDS Input/Output Compatible
- These are Pb-Free Devices



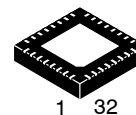
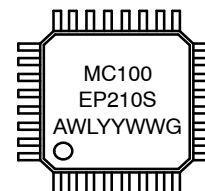
ON Semiconductor®

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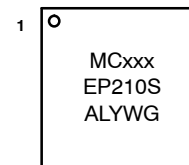
MARKING DIAGRAM*



LQFP-32
FA SUFFIX
CASE 873A



QFN32
MN SUFFIX
CASE 488AM



xxx = 10 or 100
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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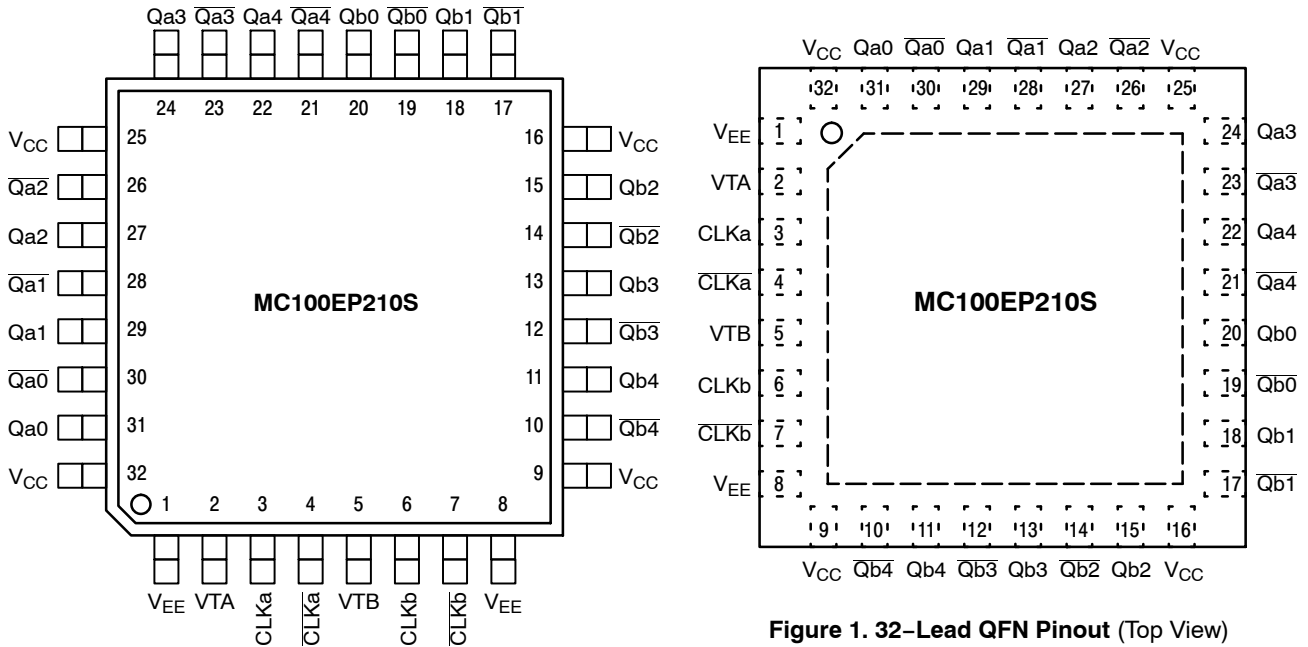


Figure 1. 32-Lead QFN Pinout (Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32-Lead LQFP Pinout (Top View)

Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|---------------------------|--|
| CLKn, \overline{CLKn} | LVDS, LVPECL CLK Inputs* |
| Qn0:4, $\overline{Qn0:4}$ | LVDS Outputs |
| VTA | 50 Ω Termination Resistors |
| VTB | 50 Ω Termination Resistors |
| V_{CC} | Positive Supply |
| V_{EE} | Ground |
| EP for QFN-32, only | The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to V_{EE} . |

*Under open or floating conditions with input pins converging to a common termination bias voltage the device is susceptible to auto oscillation.

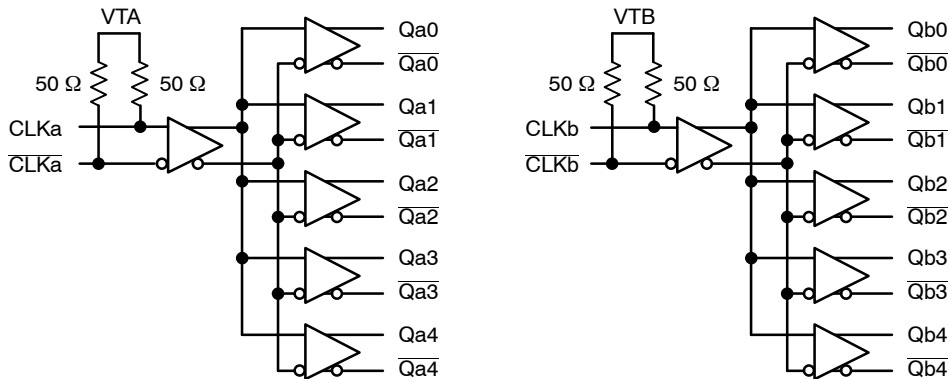


Figure 2. Logic Diagram

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Table 2. ATTRIBUTES

| Characteristics | Value | |
|---|---|-----------------------------|
| ESD Protection | Human Body Model Machine Model Charged Device Model | > 2 kV > 100 V > 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb Pkg | Pb-Free Pkg |
| | LQFP-32 QFN-32 | Level 2 Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 461 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1. For additional information, refer to Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|-------------------------|----------------------------------|-------------|--------------|
| V _{CC} | Power Supply | V _{EE} = 0 V | | 6 | V |
| V _{EE} | Power Supply (GND) | V _{CC} = 2.5 V | | -6 | V |
| V _I | LVDS, LVPECL Input Voltage | V _{EE} = 0 V | V _I ≤ V _{CC} | 6 | V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | 32 LQFP 32 LQFP | 80 55 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | 32 LQFP | 12 to 17 | °C/W |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | QFN-32 QFN-32 | 31 27 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | 2S2P | QFN-32 | 12 | °C/W |
| T _{sol} | Wave Solder | Pb Pb-Free | | 265 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 4. DC CHARACTERISTICS $V_{CC} = 2.5\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 2)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|------------|--------------|------------|--------------|------|------------|--------------|------|------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 150 | 200 | | 150 | 200 | | 150 | 200 | mA |
| V_{OH} | Output HIGH Voltage (Note 3) | 1250 | 1400 | 1550 | 1250 | 1400 | 1550 | 1250 | 1400 | 1550 | mV |
| V_{OL} | Output LOW Voltage (Note 3) | 800 | 950 | 1100 | 800 | 950 | 1100 | 800 | 950 | 1100 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| R_T | Internal Termination Resistor | 43 | | 57 | 43 | 50 | 57 | 43 | | 57 | Ω |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | CLK CLK | -150 -150 | 150 150 | -150 -150 | | 150 150 | -150 -150 | | 150 150 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with V_{CC} .

3. All loading with 100 Ω across LVDS differential outputs.

4. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. AC CHARACTERISTICS $V_{CC} = 2.375$ to 2.625 V , $V_{EE} = 0\text{ V}$ (Note 5)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-----------------------------|---|-------|----------------|------------------|------|----------------|------------------|------|----------------|------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{\text{maxLVDS/LVPECL}}$ | Maximum Frequency (See Figure 2. $F_{\text{max/JITTER}}$) | | > 1 | | | > 1 | | | > 1 | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay | 425 | 525 | 625 | 450 | 550 | 650 | 475 | 575 | 675 | ps |
| t_{skew} | Within-Device Skew (Note 6) Device-to-Device Skew (Note 7) Duty Cycle Skew (Note 8) | | 20 85 80 | 25 160 100 | | 20 85 80 | 25 160 100 | | 20 85 80 | 35 160 100 | ps |
| t_{JITTER} | RMS Random Clock Jitter | | 0.2 | < 1 | | 0.2 | < 1 | | 0.2 | < 1 | ps |
| V_{PP} | Minimum Input Swing | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r/t_f | Output Rise/Fall Time (20%–80%) | 50 | 130 | 200 | 75 | 150 | 225 | 80 | 160 | 230 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measured with 400 mV source, 50% duty cycle clock source. All loading with 100 Ω across differential outputs.

6. Skew is measured between outputs under identical transitions of similar paths through a device.

7. Device-to-Device skew for identical transitions at identical V_{CC} levels.

8. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.

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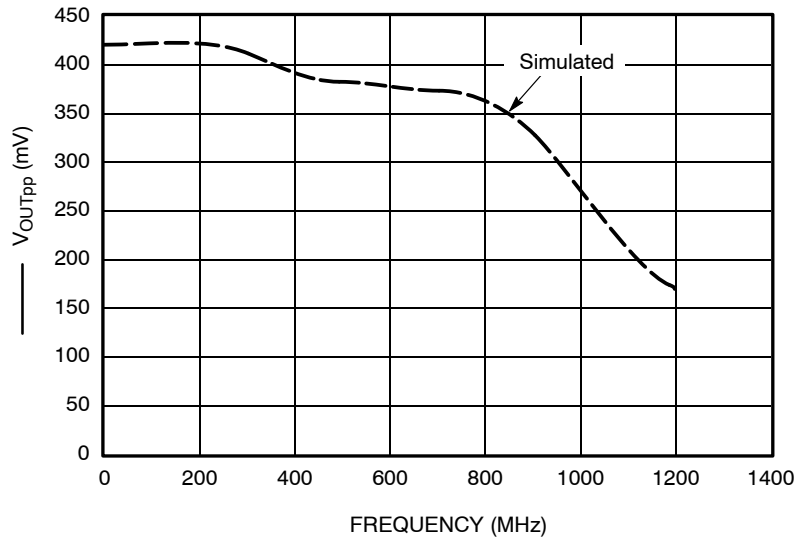


Figure 2. F_{max}

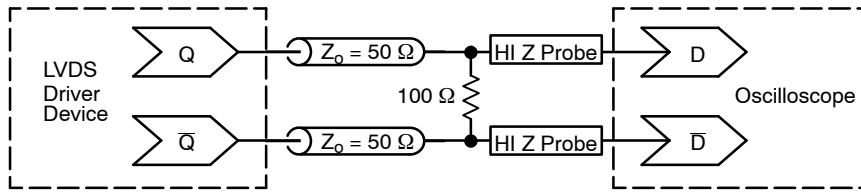


Figure 3. Typical Termination for Output Driver and Device Evaluation

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Figure 4. Tape and Reel Pin 1 Quadrant Orientation

ORDERING INFORMATION

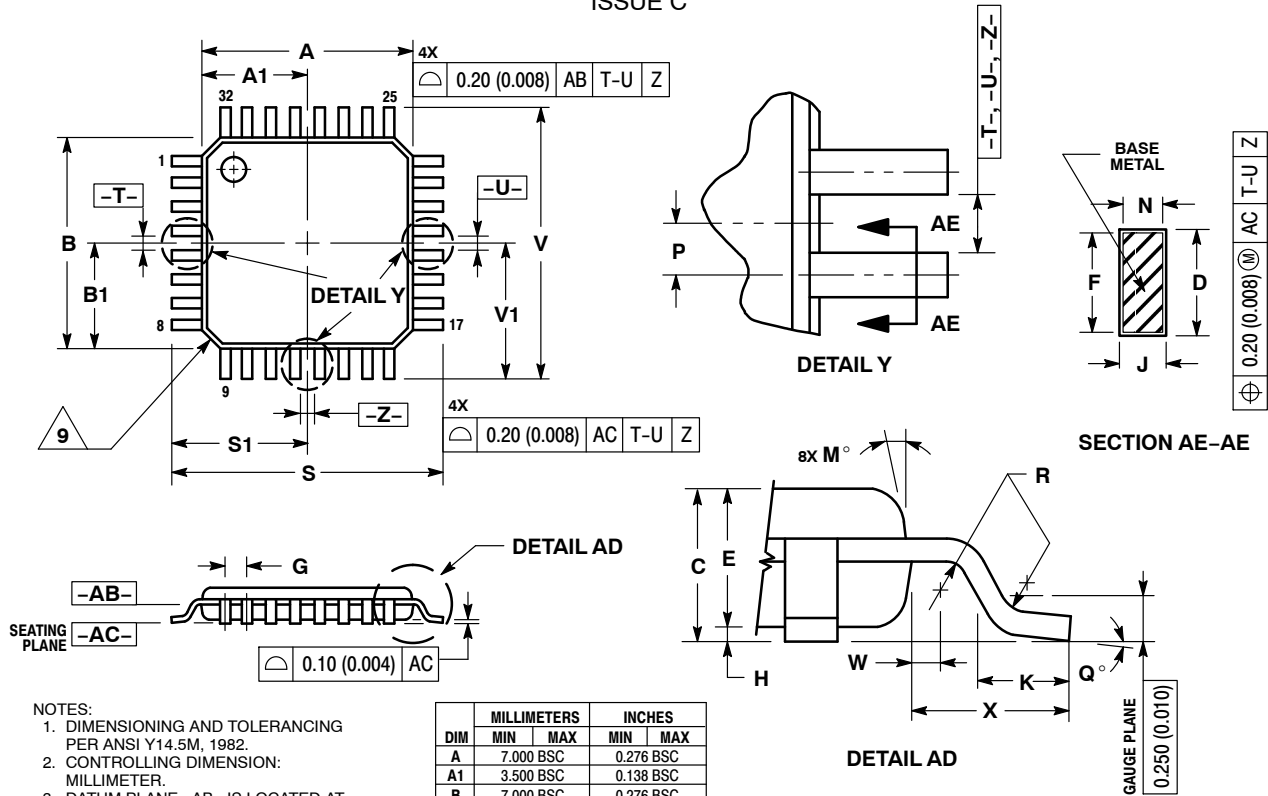
| Device | Package | Shipping [†] |
|------------------|----------------------|---|
| MC100EP210SFAG | LQFP-32 (Pb-Free) | 250 Units / Tray |
| MC100EP210SFAR2G | LQFP-32 (Pb-Free) | 2000 / Tape & Reel (Pin 1 Orientation in Quadrant B, Figure 4) |
| MC100EP210SFATWG | LQFP-32 (Pb-Free) | 2000 / Tape & Reel (Pin 1 Orientation in Quadrant A, Figure 4) |
| MC100EP210SMNG | QFN-32 (Pb-Free) | 72 Units / Tray |
| MC100EP210SMNR4G | QFN-32 (Pb-Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

32 LEAD LQFP
CASE 873A-02
ISSUE C



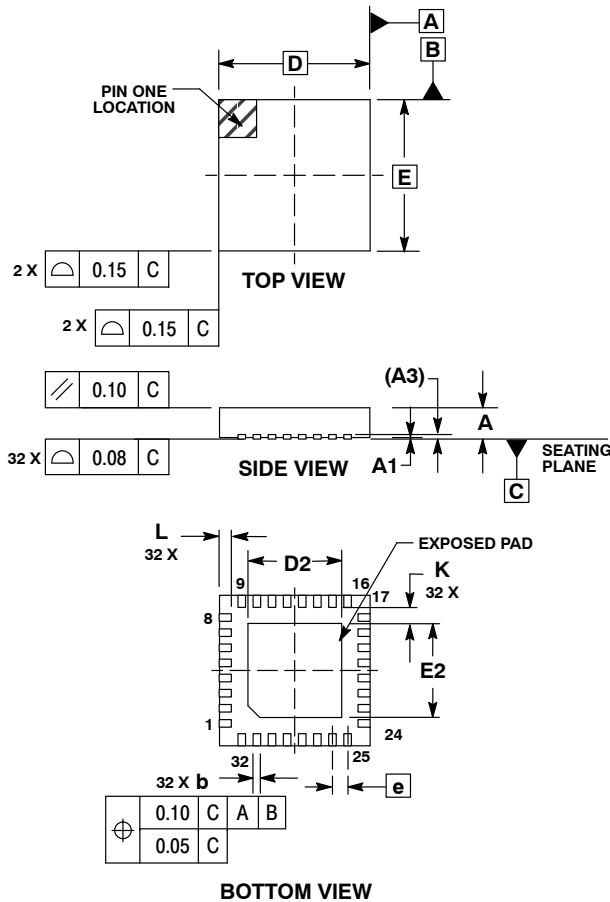
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
- DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
- MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
- EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

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PACKAGE DIMENSIONS

QFN32 5*5*1 0.5 P
CASE 488AM-01
ISSUE 0

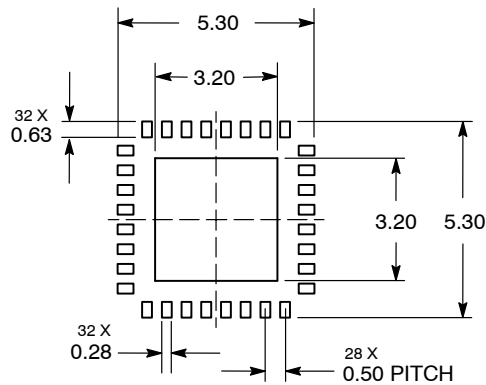


NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | | |
|-------------|-----------|-------|-------|
| DIM | MIN | NOM | MAX |
| A | 0.800 | 0.900 | 1.000 |
| A1 | 0.000 | 0.025 | 0.050 |
| A3 | 0.200 REF | | |
| b | 0.180 | 0.250 | 0.300 |
| D | 5.00 BSC | | |
| D2 | 2.950 | 3.100 | 3.250 |
| E | 5.00 BSC | | |
| E2 | 2.950 | 3.100 | 3.250 |
| e | 0.500 BSC | | |
| K | 0.200 | --- | --- |
| L | 0.300 | 0.400 | 0.500 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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